Table 2. The activities written and piloted. Summer 2017 (su17), Fall 2017 (fa17), Spring 2018 (sp18).

Activity title	Learning objectives	Pilots
Bits and numbers	• Translate integers and fixed-point numbers between bases • Express positive and negative integers in two's complement • Identify the largest and smallest integers representable using N bits	su17, fa17, sp18
Memory organization of programs	• Describe the purpose of data segment, text segment, stack, and heap memory • Draw a diagram of memory contents for an executing program • Translate object-oriented code to assembly language	su17, fa17, sp18
Stored programs	• Discuss the correspondence between assembly language instructions and binary machine code • Read the assembly language/machine code documentation • Translate arithmetic and load/store instructions between assembly language and machine code • Translate labels to addresses for branch and jump instructions	su17, fa17, sp18
Procedure calls	• Explain the importance of indirect jumps, argument registers, and return registers in procedure calls • Use procedure calling convention • Trace a recursive procedure call using memory diagrams • Write assembly code defining and calling a procedure	sp18
Combinational logic	• Convert between a truth table and Boolean equation • Write the truth table for a circuit using a switch model • Explain how a circuit-controlled switch is necessary for composability	sp18
Adders and delay	• Use truth tables to build arithmetic circuits • Explain the need for procedural reasoning in design of larger circuits like adders • Relate delay in RC circuits to a simple model for delay • Apply the simple model for delay to a combinational circuit	sp18
Adders, shifters, multipliers	• Compare the delay of various implementations of arithmetic circuits • Build variable bit shifters using various approaches • Build a multiplier from shifters and adders	su17, fa17, sp18
Sequential logic	• Identify properties of a clock signal • Write the waveform for a sequential circuit • Explain why sequential components are required in a feedback loop • Design a basic sequential circuit from a description of behavior	sp18
Addressable memory and the add instruction	• Build an addressable RAM from registers or smaller memories with fewer ports • Build a simple datapath that can execute a single instruction and program it • Modify the datapath to support a second instruction and program it	su17, fa17, sp18
Engineering digital systems	• Calculate the delay of the critical path in a synchronous circuit, and use it to determine minimum clock period and throughput • Plot and interpret a Pareto optimal curve of delay vs area • Describe the advantages and limitations of pipelining	su17, fa17, sp18